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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,519	03/01/2002	Paul T. Sasaki	X-1049 US	6632

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,519	SASAKI ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11182004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL DETAILED ACTION

1. Claims 1-45 have been examined. Claims 1, 13-17, 21, 23-27, 30-33, 35-37, 30 and 43 have been amended.

2. As a result of Applicants' amendment of 03/01/2005, the Examiner has withdrawn the claim objections.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 11/18/2005 was filed after the mailing date of the Non-Final Office Action on 11/10/2004 as a resubmission due to a typographical error. The resubmission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Arguments

4. Applicants' arguments filed 03/01/2005 have been fully considered but they are not persuasive.

<u>As per arguments for independent claims 1, 13, 24, 31, 37 and 43:</u>

The Examiner would like to point out the definition for programmable logic array, according to "The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition", page 875, is *a general-purpose integrated circuit that consists of an array of gates that*

can be programmed to perform various functions. Applicants argue that there is no teaching or suggestion in Krishna that monolithic integrated circuit 110 is a programmable logic device. The Examiner disagrees and asserts that Krishna teaches the physical m-MII interface (physical layer) is configured to divide the received packet data from the Gigabit MAC core 18 (link layer) into a group of separate data segments based on configuration control settings set by a user (programmable) in a configuration control portion 40. Krishna also teaches the configuration control 40 may be implemented as embedded microcode if the physical m-MII interface 38 is implemented as an integrated portion of a monolithic integrated circuit. By the broadest reasonable interpretation the Examiner asserts that Krishna's monolithic integrated circuit is a programmable logic device programmed by the embedded microcode and, by reference to the IEEE Dictionary definition above, is *a general-purpose integrated circuit that consists of an array of gates that can be programmed to perform various functions.* The Applicants are also reminded that during patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). See MPEP § 2111.

The remaining arguments on pages 11 and 12 for claims 1, 13, 24, 31, 37 and 43 can be summarized in the following statements: (a.) the physical layer (receiver/transmitter) is implemented in hard (application-specific) logic of the programmable logic device and the link layer is implemented using programmable logic of the programmable logic device and (b.) the CRC generator is implemented in the

physical layer of the programmable logic device. It has already been established that Krishna's monolithic integrated circuit is a programmable logic device programmed by the embedded microcode. Furthermore, Krishna teaches the monolithic integrated circuit 110 provides a completely integrated system including the Gigabit MAC 18 (link layer), the physical m-MII interface 38 (physical layer), and the physical layer transceivers 28 integrated onto a single monolithic integrated circuit 110. (Col. 7-8, lines 66,67 and 1-3). In other words, both the physical layer and link layer is implemented in the programmable logic device. Also, Krishna teaches the CRC generator is implemented in the physical layer of the programmable logic device as disclosed in the rejection of the previous of office action of record. (Col. 6, ll. 57-58). Therefore, the Examiner asserts that Krishna teaches the above stated limitations (a.) and (b.).

It is the Examiner's conclusion that independent claims 1, 13, 24, 31, 37 and 43 are not patentably distinct or non-obvious over the prior arts of record namely, Krishna et al (US-6094439). Therefore, the rejection is maintained. Based on their dependency on claims 1, 13, 24, 31, 37 and 43, claims 2-12, 14-23, 25-30, 32-36, 38-42 and 44-45, respectively, stand rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 13, 21, 24-26, 31-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Krishna et al (US-6094439), hereinafter Krishna.

Claims 13, 24 and 31:

Krishna teaches a monolithic integrated circuit 110 (application specific logic/programmable logic device as per claim 24) that provides a completely integrated system including the Gigabit MAC 18, the physical m-MII interface 38, and the physical layer transceivers 28 integrated onto a single monolithic integrated circuit 110. (Col. 7-8, lines 66,67 and 1-3). Krishna also teaches that a media access controller (MAC) layer 24 having a Gigabit MAC core 18 media independent interface (GMII) generates a data packet, also referred to as a data frame, according to IEEE 802.3 protocol and once the 802.3 data packet has been generated, the m-MII functionality (physical layer) in the MAC 24 selectively transmits at least a portion of the data packet (the data packet including at least a portion of the data frame) to at least one of the physical layer devices 26. The data packet output to a selected physical layer device 26 (a data node adapted to receive a data packet) may be an entire 802.3 data packet, or alternatively a segment of the data packet (at least a portion of the data frame). Krishna further teaches the m-MII 30 within the physical layer device 26 will perform additional signaling prior to sending the data segment on the corresponding physical layer link 32, for example by generating a separate preamble, or by appending an error code such as a cyclic redundancy check (CRC) code at the end of the data segment generated by CRC generator 70 and can be used by the receiver node 12b to detect a failure in the link. (Col. 4, lines 17-24, 33-38, col. 6, lines 62-65).

Claims 37, 40 and 43:

Krishna teaches a monolithic integrated circuit 110 (hard logic and programmable logic) that provides a completely integrated system including the Gigabit MAC 18, the physical m-MII interface 38, and the physical layer transceivers 28 integrated onto a single monolithic integrated circuit 110. (Col. 7-8, lines 66,67 and 1-3). Krishna also teaches that a media access controller (MAC) layer 24 having a Gigabit MAC core 18 media independent interface (GMII) generates a data packet, also referred to as a data frame, according to IEEE 802.3 protocol and once the 802.3 data packet has been generated, the m-MII functionality (physical layer) in the MAC 24 selectively transmits at least a portion of the data packet (the data packet including at least a portion of the data frame) to at least one of the physical layer devices 26. The data packet output to a selected physical layer device 26 (a data node adapted to receive a data packet) may be an entire 802.3 data packet, or alternatively a segment of the data packet (at least a portion of the data frame). Krishna further teaches the m-MII 30 (receiver)within the physical layer device 26 will perform additional signaling prior to sending the data segment on the corresponding physical layer link 32, for example by generating a separate preamble, or by appending an error code such as a cyclic redundancy check (CRC) code (CRC value) at the end of the data segment generated by CRC generator 70 and can be used by the receiver node 12b to detect a failure in the link. (Col. 4, lines 17-24, 33-38, col. 6, lines 62-65).

Claim 21:

Krishna teaches the physical m-MII interface 38 (physical layer), includes a CRC generator 70 also includes an elasticity buffer 52 that matches the different transmission rates between the Gigabit transmission rate of the Gigabit MAC core 18 and GMII 34, and the multiple 100 Mb links 32 (CRC generator further comprises a first module to support a first communication standard and a second module to support a second communication standard). (Col 6, lines 43-47 and 57, 58).

Claim 32 and 33:

Krishna teaches the physical m-MII interface 38 (physical layer) includes a CRC checker 44 (CRC compare circuit), which detects the presence of an error in the transmitted data frame from the Gigabit MAC 18 (link layer connected to the CRC compare circuit per claim 33) by comparing the received data with the error code appended at the end of the 802.3 frame (compare the packet CRC value to the calculated CRC value). (Col. 5, lines 38-54).

Claim 34:

Krishna teaches the physical m-MII interface 38 (physical layer) includes a CRC checker 44 (CRC compare circuit), which detects the presence of an error in the transmitted data frame from the Gigabit MAC 18 (link layer connected to the CRC compare circuit per claim 33) by comparing the received data with the error code appended at the end of the 802.3 frame (the CRC compare circuit identifies mismatches between the packet CRC and the CRC for the link layer). (Col. 5, lines 38-54).

Claim 35:

Krishna teaches the physical m-MII interface 38 (physical layer), includes a CRC checker 44 (CRC compare circuit), which can be configured to detect a fault in one of the links 32 and/or the associated transceiver 28, and to reroute traffic accordingly. Hence the routing functionality within the physical m-MII interface 38 can be configured to reroute packet data in response to a detected transmission condition on one of the links (the link layer relies upon the CRC compare circuit in the physical layer to identify the defective packets). (Col. 7, lines 51-57).

Claims 25 and 36:

Krishna teaches the physical m-MII interface 38 (physical layer), includes a CRC generator 70 also includes an elasticity buffer 52 that matches the different transmission rates between the Gigabit transmission rate of the Gigabit MAC core 18 and GMII 34, and the multiple 100 Mb links 32 (CRC generator is adapted to perform a plurality of CRC functions to support a plurality of communication standards). (Col 6, lines 43-47 and 57, 58).

Claims 38, 39, 41, 42, 44 and 45:

Krishna teaches a monolithic integrated circuit 110 (PLD/FPGA) that provides a completely integrated system including the Gigabit MAC 18, the physical m-MII interface 38, and the physical layer transceivers 28 integrated onto a single monolithic integrated circuit 110. (Col. 7-8, lines 66,67 and 1-3).

Claim 26:

This claim is rejected as per claims 13, 24 and 31 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-12, 14-20, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishna et al (US-6094439), hereinafter Krishna, in view of Matsuura et al. (US- 20040114638), hereinafter Matsuura.

Claim 1:

Krishna teaches a media access controller (MAC) layer 24 having a Gigabit MAC core 18 media independent interface (GMII), which generates a data packet, also referred to as a data frame (assembling a data frame), according to IEEE 802.3 protocol, and sends and receives these data packets to and from the physical layer. Krishna also teaches a physical m-MII interface 38 which is coupled to the physical layer links 32 via the respective physical layer transceivers 28 and is configured for receiving the packet data from the Gigabit MAC core 18 (encapsulating the data frame into a data packet). Krishna further teaches the physical m-MII interface 38 also includes a CRC generator, 70 which generates a new frame check sequence for the data segment output by the data router and can be used by the receiver node 12b to detect a failure in the link (performing a CRC on the data frame; and adding the CRC value to the data packet). Krishna even further teaches a data packet generated by the

GMII 34 according to IEEE 802.3 protocol includes a preamble 62, a data portion 64 (a data field) including the packet header and payload, and a frame check sequence field 66, for example a cyclic redundancy check (CRC) code. Krishna discloses a preamble detector 46, which detects the preamble of the data packet and identifies the beginning of a data packet from the Gigabit MAC 18 (start field identifying the start of the packet). (Col. 3, lines 66, 67, col. 4, lines 17, 18, col. 5, lines 2-5, 18-20, 38-54, col. 6, lines 12-16, lines 57-65). Krishna does not explicitly teach "appending idle data to the data packet to form a data assembly". However, Krishna does teach a data packet generated by the GMII 34 according to IEEE 802.3 protocol includes a preamble 62, a data portion 64 including the packet header and payload, and a frame check sequence field 66, for example a cyclic redundancy check (CRC) code. Matsuura teaches in an analogous art the use of IDLE codes for use in the inter-frame gap between the MAC (Media Access Control) frame, which is composed of data codes, special characters indicating the beginning and end of data and an overhead, and adjacent MAC frames are separated by a signal for synchronization, that is, by an inter-frame gap IFG (appending idle data). Matsuura teaches inter-frame gap IFG adjusts or regulates an excess or shortage of data resulting from non-coincidence between the bit rates by deletion or insertion of the IDLE2 code. (Page 4, ¶ 78, page 5, ¶ 86, 87). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Krishna's GMII with Matsuura's MAC (Media Access Control) to include the Matsuura inter-frame gap IFG (appending idle data) function. The artisan would have been motivated to do so

because this would enable Krishna to add idle data to the data packet in order to adjust the data packet size.

Claim 2-7:

Matsuura teaches that IDLE codes or use in the inter-frame gap between MAC frames there are two kinds of IDLE codes, that is, IDLE1 and IDLE2; according to the IEEE 802.3z standard, in the case where an RD (running disparity) value immediately following a second special code (i.e., Packet_Extension /R!) of first and second special codes (an octet of each of End_of_Packet and Packet _Extension indicated by /T/R/ or two octets of Packet _Extension indicated by /R/R/) (data packet includes an end-of-packet field as per claim 4) of an inter-frame gap IFG is positive as shown in FIG. 12B, the third code of the inter-frame gap is IDLE1 and the fourth and subsequent codes are IDLE2. Matsuura also teaches when the RD value immediately after the second special code /R/ of the inter-frame gap is negative, the third code of the inter-frame gap is IDLE2 and the fourth and subsequent codes are also IDLE2 (evaluating the packet assembly to obtain a disparity value as per claim 2a. and if the disparity is incorrect, changing the packet assembly/idle data as per claims 2b. and 3) where the RD value is defined such that RD=+ or RD=- or equal to the RD value of the immediately preceding 10-bit word, depending on whether the number of "1s" in the immediately preceding 10-bit word is larger or smaller than or equal to the number of "0s". Matsuura further teaches the IDLE2 code is a concatenation of a 10-bit code "0011111010" referred to as the special character K28.5 (comma character as per claim 5) and the 10-bit code 0x50. Matsuura even further teaches it is defined that the first seven bits "0011111" in the bit

sequence (comma character includes five consecutive identical bits as per claims 6 and 7) of the special character K28.5 would not occur in bit sequences by any code trains, and the character K28.5 is called a "comma character" (as per claim 5) since it is used as a delimiter in the bit sequence. (Page 4, ¶ 78, Fig. 5).

Claim 8:

Krishna teaches the data router 50 is configured for selectively transmitting at least a portion of the received packet data to at least one of the plurality of physical layer devices 28 and the CRC generator 70 generates a new frame check sequence for the data segment output by the data router (appending the idle data occurs before performing the CRC of the data frame).

Claim 9:

This claim is rejected as per claim 2-7 above.

Claims 10-12:

Krishna teaches a monolithic integrated circuit 110 (PLD/FPGA) that provides a completely integrated system including the Gigabit MAC 18, the physical m-MII interface 38, and the physical layer transceivers 28 integrated onto a single monolithic integrated circuit 110. (Col. 7-8, lines 66,67 and 1-3).

Claim 14:

This claim is rejected as per claim 1 above.

Claim 15:

This claim is rejected as per claim 2-7 above.

Claims 16-20:

These claim are rejected as per claim 2-7 above.

Claims 27 and 28:

These claim are rejected as per claim 2-7 above.

7. Claims 22, 23, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishna et al (US-6094439), hereinafter Krishna, in view of Bender et al. (EP-0676697), hereinafter Bender.

Claims 22, 23, 29 and 30:

Krishna does not explicitly teach that the "CRC generator further comprises a force-error input terminal" and "the force-error input terminal is adapted to receive a test signal for inducing the CRC generator to produce an error". However, Krishna does teaches the physical m-MII interface 38 also includes a CRC generator, 70 which generates a new frame check sequence (CRC code) for the data segment output by the data router and can be used by the receiver node 12b to detect a failure in the link. Bender teaches in an analogous art a Cyclic Redundancy Check (CRC) generator in an adapter 1 (physical layer) for generating CRC code; and a parity detector coupled to the CRC generator for detecting the parity data transmitted by the main processor to the adapter 1. Bender also teaches the parity detector includes a means for forcing the CRC generator to generate an error in the CRC code when a parity error is detected. (Col. 4, lines 37-51, col. 19, lines 52-58, col. 20, lines 6-9). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Krishna's

CRC generator to include Bender's force-error function. The artisan would have been motivated to do so because this would enable Krishna's CRC generator to have the flexibility of injecting errors into the CRC code to test the CRC checker 44.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

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